REMARKS

1. Claim 10 is amended in response to the Examiner's objection. No new matter is added.

2. Claims 1-2. 4-8, 20-21, 23-27, 30 and 34-35 are rejected under 35 U.S.C 102(b) as being anticipated by "TTCrx Reference Manual" (Christiansen). The Examiner is respectfully requested to withdraw the rejection of the claims in view of the following comments distinguishing these claims over Christiansen.

Christiansen's circuit is used in a data transmission/receiver system having two channels A and B. A clock extraction circuit (FIG. 4) derives the clock signals that a transmitter uses to control the timing of edges in a data signals conveyed by each of the two channels from the data signals themselves. A pair of programmable deskew circuits delay the extracted clock signals by adjustable amounts that are controlled by commands received by a control and data interface circuit to produce output clock signals CLK01 and CLK02 that are phase adjusted to compensate for any error in timing of the extracted clock signal phase. In such a system the skew errors in the extracted clock signals are systematic functions of the channel architectures and would normally remain constant unless the channels are altered in some way. Thus once the delays of the programmable fine deskew circuits are properly adjusted, they need not be changed in the absence of any changes to the channels that cause a change in clock signal skew, thereby requiring an adjustment to the delays provided by fine deskew circuits.

Christiansen's FIG. 10 shows one of the programmable fine deskew circuits of FIG. 4. It receives an input clock signal (in) having some period T (or T_p to be consistent with the terminology of claim 1) and produces an output clock signal (out) having the same period T_p, but the output signal is phase shifted from the input signal with a delay that is adjusted by input selection control data (sel). Thus the purpose of the fine deskew circuit is to delay an input clock signal having some period T_p by an adjustable delay to produce an output clock signal having the same period T_p but which is adjustably shifted in phase from the input clock signal. It is not the function of each fine deskew circuit to produce an output clock signal having a period that differs from T_p

The applicant's apparatus as recited in claim 1 can produce an output periodic "third pulse sequence" having a period that can differ from the period T_p of the input "first pulse sequence" because the "programmable sequencer" repetitively varies the control data input to the first and second means in a programmably adjustable manner. Referring to the applicant's

FIG. 5, programmable sequencer 58 repetitively varies control data SW(A) and SW(B) as recited in claim 1.

Christiansen (FIG. 10) shows a timing signal generator that includes "first means" (upper set of N gates, lower phase detector and upper multiplexer) for adjustably delaying an input pulse sequence (in) of period T_p with a resolution of T_p/N, and "second means" (lower set of N-1 gates, lower phase detector and lower multiplexer) for adjustably delaying the output sequence of the first means with a resolution of T_p/M where M = N-1. However Christensen does not teach or suggest the "programmable sequencer" recited in claim 1. The Examiner suggests that the programmable sequencer is somehow included in the "programmable fine deskew unit" of Christiansen's FIG. 10, but while the programmable fine deskew unit of FIG. 10 includes two delay means (or stages), it does not include any programmable sequencer for producing the data (sel) selecting the delay of each stage "in response to edges of the first pulse sequence (in) as recited in claim 1 . Christensen (paragraph immediately above FIG. 10) teaches that the data (sel) for controlling the deskew unit is provided via commands the A and B channels and does not teach or suggest that it could or should be produced by a programmable sequencer of the type recited in claim 1 which changes the data in response pulses of the first pulse sequence (in).

Would one of skill in the art be motivated to use such a programmable sequencer to control the data input to the upper and lower multiplexers of Christensen's FIG. 10? First, note that the programmable sequencer of claim 1 varies the control data so that the applicant's apparatus can produce an output sequence having a period that differs from the period T_p of the input sequence. In the context of the application contemplated by Christensen, the purpose of the fine deskew circuit is to delay an input clock signal having some period T_p by an adjustable delay to produce an output clock signal having the same period T_p but which is adjustably shifted in phase from the input clock signal. It is not the function of Christiansen's fine deskew circuit in the contemplated to produce an output signal having a period that differs from that of the input signal.

Second, note that Christensen's circuit would not work properly if the control data input to the upper and lower multiplexers varied in some repetitive manner in response to pulses of the input (in) signal as recited in claim 1. Christiansen's "second means" of FIG. 10 can only delay the output sequence of the "first means" (i.e. the output of the lower multiplexer) with a resolution of $T_p/(N-1)$ when the input control data (sel) to the upper multiplexer is constant. The delay of each of the N-1 delay elements of Christiansen's "second means" is control by the lower phase lock loop

controller and the controller can only set the delay of each element to $T_p/(N-1)$ if the output signal of the upper multiplexer has a constant period T_p. If the second means input signal does not have a constant period T_p as a result of variations in the sel input to the upper multiplexer, than the second circuit delay resolution will not be $T_p/(N-1)$. Note that depending on the manner in which the data input to the first multiplexer varies, the lower phase lock loop controller could become unstable. Thus one of skill in the art would not consider using such a programmable sequencer to control Christiansen's fine deskew unit.

Christiansen therefore fails to teach or suggest the programmable sequencer recited in claim 1 since such a programmable sequencer would cause Christiansen's fine deskew unit to operate in a manner inconsistent with its intended purpose, and could cause Christiansen's fine deskew unit to become unstable.

Claims 1-2, 4-8, 20-21, 23-27, 30 and 34-35 are patentable over Christiansen for similar reasons.

3. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen. The Examiner is respectfully requested to withdraw this rejection in view of the following comments distinguishing these claims over Christiansen.

Claim 3 recites that at least one of the first and second ranges is wider than T_p. In Christiansen's circuit of FIG. 10 the first and second ranges are both T_p. The Examiner incorrectly takes "Official Notice that it is well known to have at least one of the first and second range be wider than T_p in order to compensate for delay variations due to imperfections...and environment..." The applicant challenges such Official Notice, respectfully requesting the Examiner to provide prior art showing that it is well-known to adapt a two-stage delay circuit of Christiansen's architecture so that each stage has a delay range wider than the period T_p of its period input signal.

Christiansen does not teach that the two stages could or should have ranges above T_p, and the Examiner provides no evidence that anyone other than Christiansen has contemplated such a two-stage delay circuit, and does not indicate <u>how</u> Christiansen's circuit could be adapted to increase the range of its two delay stages beyond T_p. Moreover, the Examiner's employs incorrect reasoning as to <u>why</u> one of skill in the art might want to increase the range of each of Christensen's delay stages. With the range of each of Christiansen's delay stages exactly T_p (the period of its input signal), the resolution of the circuit (i.e., the resolution with which it can compensate the phase of the input clock signal for delay variations) is $(Tp/N)-Tp/(N-1)$.

Increasing the range of either or both circuits to be larger than T_p would have no effect on its ability to compensate for variations in input signal (in) delay. Thus one of skill in the art would not be motivated to increase the delay ranges of Christensen's two delay stages beyond T_p since it would serve no purpose and since neither Christensen nor any cited prior art teaches or suggests doing so.

Claim 22 is patentable over Christiansen for similar reasons.

4. Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38 are rejected under U.S.C. 103(a) as being unpatentable over Christiansen in further view of U.S. Patent 6,388,485 (Kim). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following arguments distinguishing them over the combination of Christiansen and Kim.

For the reasons cited above in section 2, the Examiner incorrectly relies on Christiansen as teaching the portion of the subject matter of these claims generally similar to that recited in claim 1 and relies on Kim only as teaching the remaining portions of the subject matter of these claims. Thus claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38 are patentable over the combination of Christiansen and Kim for the reasons cited above in section 2.

Claim 9 recites that the "second means" comprises a series of M second gates (see gates 62 of the applicant's FIG. 7) and a series of M third gates (see gates 68 of the applicant's FIG. 7). The second gates receive the "third pulse sequence" (CLOCK) while the third gate receives the "first pulse sequence" (ROSC). Christensen's FIG. 10 shows only the "second gates" (i.e. the lower series of gates) and does not show the recited third series of gates. The Examiner therefore cites Kim's circuit 30 of FIG. 3 as disclosing the recited "second means" and suggests that it would be obvious to modify Christian's circuit to use Kim's circuit 30 in place of the "N-1" stage of Christiansen's FIG. 10.

Kim's circuit 30 has two delay stages 326 and 344, each of which receives the same periodic signal (ECLK) as input. The applicant concedes that the two delay stages could be formed by separate series of gates, however the applicant's claim 9 indicates that the "second means" includes second gates in series receiving the second pulse sequence and third gates in series receiving the first pulse sequence. Thus in the applicant's claim 9, the first gates and second gates receive different periodic input signals, whereas in Kim's circuit 30, the first gates (326) and second gates (344) receive the same periodic input signal ECLK. Note that the applicant's "second means" as exemplified by the applicant's FIG. 7 has two periodic input signals ROSC and clock (i.e., the recited "first pulse sequence" and "second pulse sequence")

whereas Kim's circuit 30 has only a single input signal ECLK. Hence Kim fails to teach the applicant's "second means" as recited in claim 9.

Claims 10, 12-14, 17-19, 28-29, 31-33, and 36-38 are patentable over the combination of Christiansen and Kim for similar reasons.

In view of the foregoing amendments and remarks, it is believed that application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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